REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of the above referenced application is respectfully requested.

Claims 24-52 stand rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have been amended to overcome this rejection.

Claims 48 and 49 stand rejected under 35 USC §103 (a) as being unpatentable over Vicard in view of Hong.

Claim 51 stands rejected under 35 USC §103 (a) as being unpatentable over Vicard in view of what was well known in the art.

Claims 24-42, 44-47, 50 and 52 stand rejected under 35 USC §102 (e) as being anticipated by Vicard et al, U.S. Patent No. 6,003,105 B1. With regards to independent Claim 24, the '105 patent to Vicard is rather thin in detail and it is believed that acknowledgments are required between data transactions. Applicant reserves the right to argue this in detail later, no concession on this rejection is made. None the less, Applicant has rewritten independent Claim 24 to focus on a related novel aspect of the present invention, namely, a circuit sending, during a data transaction, an address and then proceeding, without waiting, to a data cycle to serially send the data. Support for this limitation is found in Applicant's specification on page 19 lines 20-24. The present invention achieves technical advantages by avoiding latency, such as that which exists in the teachings of Vicard of '105. Specifically, Vicard teaches first buffering an address

and the data, and then sending this information. With regards to a PCI bus in particular, latency will choke a PCI bridge interface. It is notable that Vicard does not address burst data transactions or latency during or between transactions, which is a good example of where the present claimed invention achieves technical advantages. When sending data during burst transactions such as a multiple read or multiple write, Vicard teaches buffering the address and data before sending either. This creates latency, particularly because these buffers will need to be cleared before accepting another data transaction. In contrast, the present invention uses FIFO's such that during a data transaction an address and data is sent out as quick as it is received. With emphasis, Vicard does not send an address, and then without waiting, data. Accordingly, independent Claim 24 is believed to be allowable over the cited prior art of record, and a notice to this effect is respectfully requested. Independent Claim 31 has been similarly amended. The remaining claims 25-30 and 32-53 all ultimately depend from independent Claim 24 or 31, and are believed to be allowable for the foregoing reasons as well.

ALLOWABLE SUBJECT MATTER

Claim 43 is indicated as allowable over the prior art if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 54-59 are indicated as allowed.

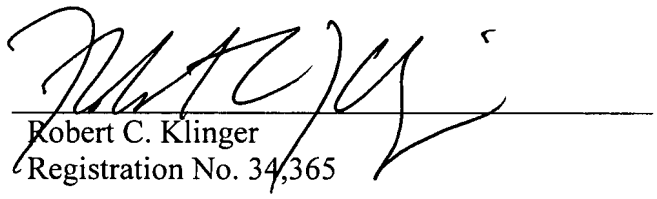
A Request for Continued Examination is included herewith along with the requisite fee of $790.00. A Three Month Extension of Time is included herewith along with the requisite fee of $1,020.00.

A change of correspondence address has also been included.

No additional fees are believed to be due, however, the Examiner is authorized to debit Applicant's Deposit Account #10-0096 if any additional fees are required.

If the Examiner has any further issues, the Examiner is encouraged to contact the undersigned to resolve these matters by phone where possible.

Respectfully Submitted,



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